CLAIMS

1. A system mounting a semiconductor die within a package comprising:

a mounting surface;

an X-lead frame coupled to said mounting surface, and

wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said semiconductor die.

2. A package as described in Claim 1 wherein said semiconductor die is a power enhancement mode JFET having a surface region defining a source, a surface region defining a drain and a surface region defining gate.

3. The power semiconductor package of Claim 2 wherein electrical coupling between said drain and said X-lead frame is realized by angular projections of said X-lead frame contacting said drain.

4. The power semiconductor package of Claim 2 wherein said X-lead frame is bonded to a first terminal disposed on said mounting surface.

5. The power semiconductor package of Claim 2 wherein a second terminal disposed on said mounting surface is electrically connected to said source.

6. The power semiconductor package of Claim 2 wherein a third terminal disposed on said mounting surface is electrically connected to said gate.

7. The semiconductor package of Claim 1, wherein said package is sized and shaped to conform to an S08 configuration.

8. The semiconductor package of Claim 1, wherein said first terminal is a solid terminal spanning the full width of four leads and the spaces between four leads on one side of said S08 package.

9. The semiconductor package of Claim 1, wherein said second terminal is a solid terminal spanning a width of three leads and the spaces between three leads on a side of said S08 package opposite to said first terminal.

10. The semiconductor package of Claim 1, wherein said third terminal is a solid terminal spanning a width of a single lead on a side of said S08 package opposite to said first terminal.

11. A power semiconductor package comprising:

a bottom mounting surface having at least one first terminal extending from said bottom mounting surface;

at least one second terminal extending from said bottom mounting surface being co-planar with said first terminal;

at least one third terminal extending from said bottom mounting surface being co-planar with said first terminal;

a semiconductor power enhancement mode JFET die having a top surface defining a drain connection and a bottom surface on which a first metalized region defining a source and a second metalized region defining a gate are disposed, said top surface being coupled to an X-lead frame such that said first terminal is electrically connected to said drain;

a first conductive region disposed on said mounting surface such that said second terminal is electrically connected to said source, and

a second conductive region disposed on said mounting surface such that said third terminal is electrically connected to said gate.

12. The power semiconductor package of Claim 11 wherein electrical coupling between said drain and said X-lead frame is realized by angular projections of said X-lead frame contacting said drain.

13. The power semiconductor package of Claim 11 wherein said X-lead frame is bonded to said first terminal.

14. The power semiconductor package of Claim 11 wherein said package is sized and shaped to conform to an S08 configuration.

15. The power semiconductor package of Claim 11 wherein said first terminal is a solid terminal spanning the full width of four leads and the spaces between four leads on one side of said S08 package.

16. The power semiconductor package of Claim 11 wherein said second terminal is a solid terminal spanning a width of three leads and the spaces between three leads on a side of said S08 package opposite to said first terminal.

17. The power semiconductor package of Claim 11 wherein said third terminal is a solid terminal spanning a width of a single lead on a side of said S08 package opposite to said first terminal.

18. The power semiconductor package of Claim 11 wherein said package includes a plastic housing that substantially encapsulates said bottom mounting surface, said X-lead frame and said JFET die.

19. The power semiconductor package of Claim 11 wherein said JFET die is disposed between said X-lead frame and said mounting surface without bonding to said JFET die.

20. A power semiconductor housing comprising:

a power enhancement mode JFET die having a top surface defined as a drain, a first bottom surface region defined as a source and a second bottom surface region defined as a gate;

an X-lead frame bonded to a first lead on a mounting surface and forming electrical coupling between said drain and said first lead by means of angular extensions of said X-lead frame contacting said drain;

a second lead on said mounting surface contacting said first bottom surface region providing electrical coupling with said source;

a third lead on said mounting surface contacting said second bottom surface region providing electrical coupling with said gate, and

wherein said first lead, said second lead and said third lead are coplanar on said mounting surface.

21. The power semiconductor housing of Claim 20 wherein said housing is sized and shaped to conform to an S08 configuration.

22. The power semiconductor housing of Claim 20 wherein electrical contact between said first lead and said drain, said second lead and said source, and said third lead and said gate are completed without bonding between surfaces.